Agilent
PCI Express® Design and Test – From Electrical to Protocol

Computing

Front Side Bus, Digital Video, Memory Bus, I/O

Enterprise

Storage, LAN

Aerospace/Defense

Sat/Communications

Digital Home

Video Consumer

Communications

Wireless/Digital Wireless

Thoroughly characterize and validate PCI Express designs

Agilent Technologies

Realize Your Best Design

In digital standard, every generation change puts new risks in your path. We see if firsthand when creating our products and working with engineers like you. Agilent's solution set for high-speed digital test is a combination of instrumentation and broad expertise built on our early and ongoing involvement with industry experts.

PCI Express® technology has been implemented broadly in systems requiring high-speed data transfer, such as video or graphics. Initially embraced by high-performance desktop and server systems, it is now finding a home in embedded applications. Specifications and compliance tests are defined by the PCI Special Interest Group (PCI-SIG®) (see Figure 1).

The overwhelming concern for designers is interoperability and backward compatibility. You need tools to validate the parametric and protocol aspects of your designs to make sure your design is in compliance, and to see how close the design performance is to specification.

Higher data rates increase signal integrity symptoms like reflections and crosstalk, causing signal degradation and timing issues. A shorter clock cycle means a smaller jitter budget, so reducing jitter is far more complex.

Likewise, as PCI Express is used in more diverse environments, the protocol layer capabilities are increasing.

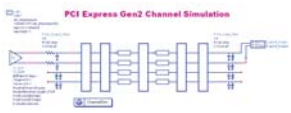
When you can gain insight to your design early in the design cycle, you can take corrective action quickly to make sure you meet product quality, interoperability and time-to-market goals. By sharing our latest experiences, we can help enhance your ability to create products you'll be proud of. Work with Agilent- and realize your best design.

PCI Express version	1.0a	1.1	2.0	3.0
Specification released	2003	2005	2007	2010
Data transfer rate	2.5 GT/s	2.5 GT/s	5.0 GT/s	8.0 GT/s
Data fundamental frequency	1.25 GHz	1.25 GHz	2.5 GHz	4.0 GHz
Data encoding	8b/10b	8b/10b	8b/10b	PRBS23 Scrambling
Total bandwidth for x16 link	~6.4 GB/s	~6.4 GB/s	~12.8 GB/s	~25.6 GB/s
Key changes	Initial release	Tighter jitter and reference clock tests	Speed, Cable specification, PLL bandwidth test, tighter jitter and reference clock tests, new de-emphasis levels	Speed, higher PLL bandwidth, more complex de-emphasis, scrambling, others still being decided

Figure 1. PCI Express technologies and key specifications

Key Task

PCI Express design can be segmented into physical layer, data link layer and transaction layer. The PCI-SIG provides the Compliance Base Board (CBB), the Compliance Load Board (CLB), and the SigTest software to facilitate electrical compliance testing. Protocol compliance requires a different approach. While the PCI-SIG workshops provide a formal verification of your design, you need to perform compliance tests before attending a workshop. Only Agilent offers solutions to meet your needs in the electrical physical layer, protocol layer, and functional test (see Figure 2).

Physical layer: interconnect design	Physical layer: transmitter test	Physical layer: receiver test	Data link/ transaction layer
			

• ADS Design Software	• 90000A Series oscilloscope
	• N5393C PCI Express electrical compliance software
	• EZJIT plus and High-speed serial data analysis software
	• 86100C DCA-J
		• J-BERT N4903B high-performance serial BERT
		• 81250 ParBERT
		• N4916A de-emphasis signal converter
		• N5990A Automated compliance and device characterization test software
			• E2960 Protocol test solution for PCIe 1.0 and 2.0
			  • PCIe analyzer
			  • PCIe exerciser
			  • PCIe jammer
			  • Protocol compliance test card (PTC)
			• U4300 Series digital debug console for PCIe 3.0, 2.0, and 2.0
			  • PCIe analyzer
			  • PCIe exerciser
			  • Probing

			
• 86100C DCA-J/TDR • N5230C PNA-L network analyzer			

Figure 2. Agilent PCI Express design and test solutions

Applying expertise

Agilent has decades of experience in digital, RF and protocol engineering. We understand the reflections, insertion and return loss, jitter budget, timing margins and other issues that designers have to face in high data rate standards. Our protocol expertise is leveraged from our long time support of the PCI standards. As an active member of the PCI-SIG, with consistent participation in workshops and specification issues, Agilent has a solid understanding of the physical layer, data link layer and transaction layer used by PCI Express.

Agilent has a long history of collaborative innovation with industry leaders. It puts Agilent in a position to develop tools that meet the physical challenges, are customized to the needs of the standard, and are relevant to the way designers and developers need to use them.

Complete, reliable test coverage

What makes Agilent solutions so compelling is that they are the best tools, in every category, to meet the challenges presented by PCI Express. They were developed to match the application's specific needs – oscilloscopes to verify signal integrity and jitter, BERTs and pattern generators to create complex stimulus signals (see Figure 3), protocol exercisers/analyzers to debug packets, time-domain reflectometer (TDR) and a vector network analyzer (VNA) to characterize impedance, and EDA software to simulate designs.

The quality of Agilent solutions is the key to easier, faster and more confident testing of your PCI Express designs. Accurate results reduce the number of design cycles to help you get to market faster, and they ensure robust designs that uphold your competitive advantage in the market.

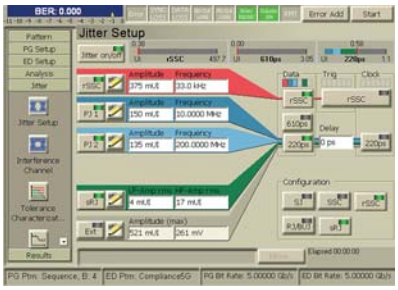


Figure 3. Agilent J-BERT N4903B produces calibrated jittered signals for stress testing

Agilent gets involved, you benefit

What makes Agilent solutions so compelling is that they are the best tools, in every category, to meet the challenges presented by PCI Express. They were developed to match the application's specific needs – oscilloscopes to verify signal integrity and jitter, BERTs and pattern generators to create complex stimulus signals (see Figure 3), protocol exercisers/analyzers to debug packets, time-domain reflectometer (TDR) and a vector network analyzer (VNA) to characterize impedance, and EDA software to simulate designs.

The quality of Agilent solutions is the key to easier, faster and more confident testing of your PCI Express designs. Accurate results reduce the number of design cycles to help you get to market faster, and they ensure robust designs that uphold your competitive advantage in the market.

Validating PCI Express performance involves characterizing the reference clock and data signals. Your product must successfully pass "Gold Suite" testing -- a superset of what the PCI-SIG SigTest tests -- at a PCI-SIG workshop using the official PCI-SIG approved test fixtures. Key parameters are rise-time, amplitude, eye width, jitter and Phase-Locked Loop (PLL) bandwidth and peaking.

Measure quickly, with confidence

Whether you are troubleshooting, capturing contiguous waveforms, ensuring correct operation, or proving compliance, an oscilloscope with low noise, low jitter, and high probe accuracy is critical for measurement accuracy. Eye diagram tests examine the minimum eye opening for adequate operation. Reference clock jitter analysis helps ensure that the system bit error ratio (BER) can be achieved.

Agilent's Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter by a real-time oscilloscope in the industry. The N5400A EZJIT Plus jitter software includes the SigTest clock recovery algorithm for accurate results. The E2688A high-speed serial data analysis software provides eye diagrams, eye mask testing, and failure analysis tools (see Figure 4). Add the Agilent N5393C PCI Express electrical performance compliance and validation software to simplify setup, perform compliance tests, and produce an HTML report, complete with screenshots, to easily share your results (see Figure 5).

Precise PLL loop bandwidth analysis

To ensure interoperability, it is necessary to control the PLL loop bandwidth of your design. Accurate characterization of PLL loop bandwidth and peaking requires a receiver, such as an oscilloscope, that can accurately measure injected sinusoidal jitter. An alternative approach is to use a spectrum analyzer and signal generator to sweep the PLL response.

The Agilent 86100C Infiniium DCA-J wideband oscilloscope mainframe with the 86108A precision waveform analyzer module offer the industry's lowest intrinsic jitter of <60 fs. The 86108A hardware clock recovery circuit features a differential phase detector to demodulate the incoming jitter, which is post-processed by the 86100CU-400 PLL and jitter spectrum measurement software to measure phase noise and jitter transfer function directly (see Figure 6). This approach is used in the PCI-SIG Gold Suite to fully characterize device PLLs for conformance to specification.

The Agilent Infiniium 90000 Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter by a real-time oscilloscope in the industry.

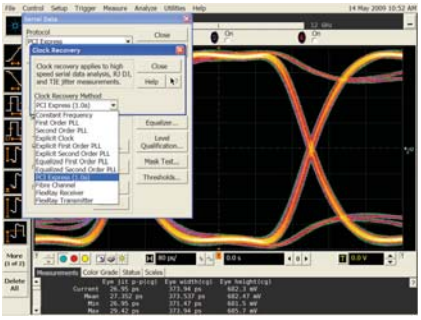


Figure 4. Real-time eye measurements using the SigTest clock recovery algorithm on 90000 Series Infiniium real-time oscilloscope

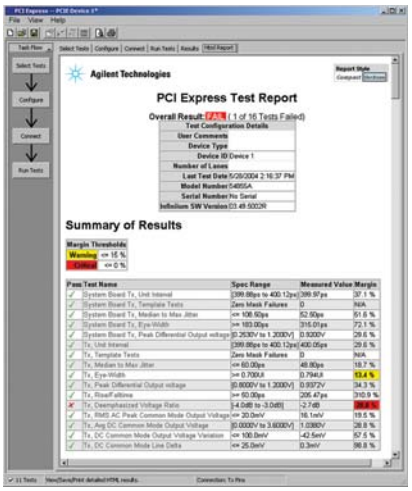


Figure 5. N5393B PCI Express electrical test software generates a summary report for your device quickly, including waveforms and the margin of the result to provide further insight

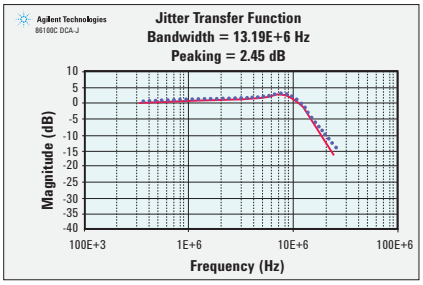


Figure 6. PLL loop bandwidth test with the 86100C DCA-J and 86108A precision waveform analyzer

The receiver in a digital transmission system must extract the digital content from its input signal with a very low bit error ratio. It typically sees a heavily degraded signal due to the channels high-frequency loss characteristics. A robust receiver must tolerate these distorted signals and make the correct bit decisions. PCI Express uses a jitter tolerance test, based on stressed eye measurements, to qualify receiver performance.

Quick, accurate jitter tolerance test

To fully characterize a receivers' jitter tolerance, you need a pattern generator to create signals to bring the device into loop-back mode, generate a reference clock with spread-spectrum capability, and create calibrated, compliant jitter injection and de-emphasis to emulate receiver stress conditions. Measurement accuracy will be determined by your ability to control these signal attributes. The more precise the source, the better the understanding of your receiver design.

The Agilent J-BERT N4903B high-performance serial BERT offers fully integrated and calibrated precision jitter sources. It provides quick, authentic, worst-case jitter and amplitude signals, including random, sinusoidal, and periodic jitter, plus Inter-Symbol Interference (ISI) to emulate motherboard conditions. The built-in jitter tolerance test routines let you quickly test your receiver (see Figure 7). When combined with the Agilent N4916A de-emphasis signal converter, you can emulate a transmitter with de-emphasized PCI Express signals to further characterize your receiver (see Figure 8).

Simplifying complex tasks

With PCI Express, its versatility shows when you create multi-lane designs. Additional lanes increase throughput, but complicate receiver design and debug. Are you able to emulate multi-lane signals? Do you have to test each lane separately, or is there a way to automate the process?

The Agilent 81250 ParBERT is a modular BERT platform that can be configured with multiple data generators and data analyzers for multi-lane testing. You can automate the receiver test, or create a complete transmitter/receiver compliance test, with the N5990A test automation software (see Figure 9). It controls the J-BERT N4903B, 81250 ParBERT, 90000 Series Infiniium oscilloscopes and other Agilent solutions.

The Agilent J-BERT N4903B has fully integrated and calibrated precision jitter sources for automated jitter tolerance testing.

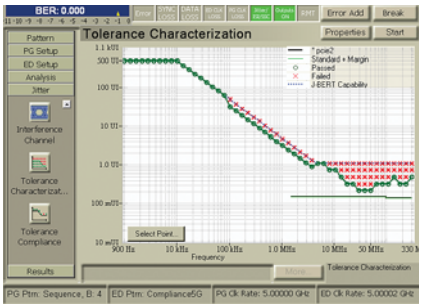


Figure 7. A jitter tolerance measurement using the J-BERT N4903B with sinusoidal jitter from 1 kHz to 300 MHz

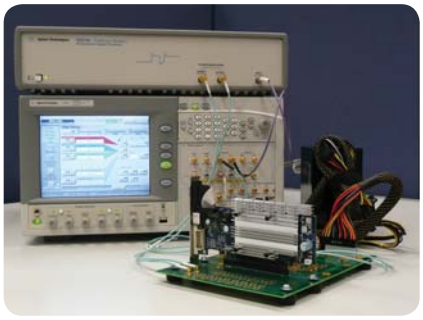


Figure 8. Jitter tolerance test setup using the J-BERT N4903B and N4916A de-emphasis signal

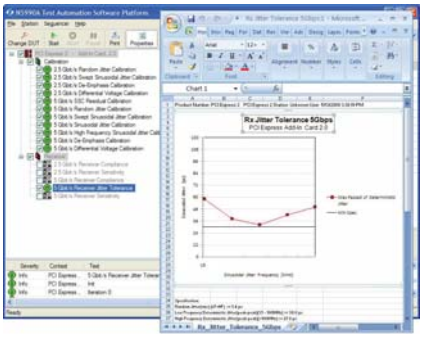


Figure 9. Automated PCI Express receiver test using the N5990A test automation software

Physical layer: interconnect design

As data rates increase, you need to pay special attention to your board design to minimize signal integrity problems. Long trace lengths cause signal attenuation, rise-time degradation, and jitter. Impedance transitions between a trace and via can cause reflections and crosstalk. You need to use tools that are more commonly used by high-frequency engineers – a time-domain reflectometer (TDR), a vector network analyzer (VNA), and high-frequency simulation software.

Accurate impedance measurements

Crosstalk, attenuation, impedance and frequency response are commonly measured using either a TDR or a VNA. To ensure optimum accuracy, these instruments employ a calibration sequence to remove the effects of any cables or fixtures that connect the TDR or VNA to the device under test.

The Agilent 86100C Infiniium DCA-J with the 54754A differential TDR/TDT module provides a quick, intuitive view of impedance discontinuities. By switching to frequency mode, you can examine the calibrated S-parameters for transmission and impedance performance of channels, cables, and connectors (see Figure 10).

The Agilent N5230C PNA-L network analyzer is based on frequency domain analysis and includes a built-in swept source and a four-port test set for differential measurements up to 20 GHz. A VNA offers higher accuracy than a TDR due to its higher dynamic range and more complete calibration approach, which is important when measuring low insertion loss or low reflection devices.

Predict interconnect performance through simulation

High-frequency engineers commonly use RF simulation tools to predict the effects of transitions, connectors, and traces. Digital designers instead rely upon SPICE-based simulators to account for analog effects. These simulators can sometimes include high-frequency S-parameter data, but rarely match an RF simulator in accurately predicting the high-frequency impact of every element in their circuit.

The Agilent Advanced Design System (ADS) has several features optimized for the high-speed digital designer. Design guides provide a quick vehicle to start a PCI Express design. You can analyze complete serial links by co-simulating individual components, each at its most appropriate level of abstraction: link, circuit or physical level (see Figure 11). Import measured S-parameters as circuit elements for more accuracy. Make analyses quickly with a user interface leveraged from Agilent oscilloscopes to display eye diagrams and jitter analysis, thereby reducing product design cycles.

To improve accuracy, the 86100C TDR utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system.

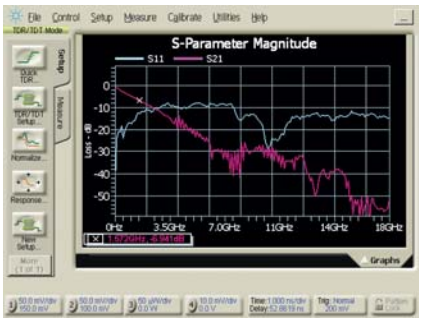


Figure 10. S-parameters can be automatically generated from the 86100C Infiniium DCA-J TDR measurement software

Agilent Technologies

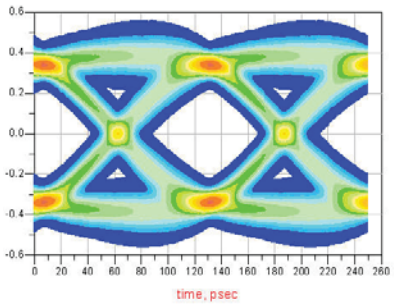


Figure 11. ADS simulates a PCI Express 3.0 channel, with the resultant differential eye measurement

Data Link/Transaction Layer: Protocol Validation and Stress Test

Protocol validation occurs at the physical layer, data link layer and transaction layer, each having its own challenges. Validation requires generating the appropriate stimulus – emulating a root-complex when testing an add-in card, or an end device for testing a root-complex device. The PCI-SIG stipulates the use of a Protocol Test Card (PTC) for the mandatory tests, but you will likely want to characterize your design more extensively to ensure interoperability.

Validate protocol quickly and easily

In addition to the mandatory protocol compliance tests, the PCI-SIG recommends over a hundred more to properly characterize your design. A key area of test is Link Training and Status State Machine (LTSSM). It is responsible for establishing the link between two components; ensuring that the link is established, and that the parameters are negotiated and agreed between the two components. With many states and sub-states, it is important to ensure that each of the state transitions is tested.

The Agilent LTSSM exerciser can help you quickly validate complex and hard to test transitions of the LTSSM in your design, including dynamic link width changes (see Figure 12). The same hardware can also be used as the exerciser for PCIe. Agilent's PCIe exerciser can emulate both root-comple and endpoint to allow testing of any type of DUT for PCIe 3.0, PCIe 2.0 and PCIe 1.0. With controllable packet generation and error insertion, the exerciser is crucial to fully validating the design of your device (see Figure 13).

How robust is your design?

Your system seems to be working, but you can't reproduce an intermittent failure. You need it to be more robust and recover from all errors correctly. This is challenging given the need to reduce validation time and the difficulty of emulating a real-life setup. Ideally you want to inject errors into real-life traffic, see how your design responds, and improve the software accordingly.

The Agilent U4305A PCI Express Exerciser can be used to replace a device on the link. Insert it into a working system, and start testing. Detailed reporting helps clearly define the source of problem for faster debug (see Figure 14). Integrate with the U4301A protocol analyzer for deep root cause analysis.

The Agilent PCI Express Exerciser can be used to replace a device on the link. This is especially important for early adoptors of PCIe 3.0

Figure 12. Configuring LTSSM tests is quick and easy with the LTSSM exerciser for PCIe 3.0 and PCIe 2.0

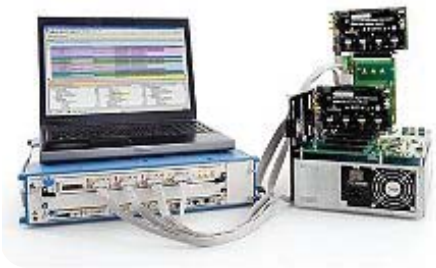


Figure 13. Thoroughly calibrate the device under test (DUT) with Agilent's exerciser.

Figure 14. Effective presentation of protocol interactions from physical layer to transaction layer

Data Link/Transaction Layer: Protocol Debug

When protocol errors are detected, you need to analyze why, then correct them. To do this, you need to access the signals, trigger on specific events, capture the traffic reliably, and view the results for quick interpretation. At speed, in-system test requires high-performance probing solutions combined with a versatile protocol analyzer.

Quickly find and solve protocol issues

Debugging PCI Express protocol means capturing traffic at speed and during power management transitions. A protocol analyzer will need to lock onto traffic quickly, then trigger on a unique protocol sequence. Debugging lower level problems such as power management, requires exceptionally fast lock times. Once you capture the traffic, you'll want to view the data at different levels of abstraction to assess what is happening.

The Agilent PCI Express protocol analyzer is a powerful tool for debug. The analyzer works with x1 to x16 designs, with advanced triggering capabilities to reduce the time needed to detect difficult-to-find errors (see Figure 15). Use the lane or packet views to observe data to find issues associated with entering and exiting out of low-power states (see Figure 16). For higher layer problems, such as data integrity, the transaction viewer lets you observe all the data from multiple completions together in one location for easy analysis.

Accessing signals for real-time debug

A key challenge in PCI Express protocol debug is gaining access to the signals in a non-invasive manner. Where you probe, and how you probe, are dependent upon your system design. Mid-bus probes provide access to traffic, but should not impact signal quality. Slot interposers need to pass signals passively over a long trace and not change the signals.

Agilent's PCI Express protocol analyzer provides a wide range of probing solutions. Agilent's Gen2 analyzer, has full size and half size mid-bus probes, slot interposers and multiple flying leads probes to access the signal.

Agilent's Gen3 probes utilizes Agilent's unique ESP (Equalization Snoop Probe) technology, with the ability to tune the equalization algorithm used according to the type of channel the analyzer is monitoring. This ensures that the data captured in the analyzer is exactly what is on the wire. Without this capability, at 8GT/s, there is a high likelihood of misrepresentation of the data on the bus, which can lead to wasted hours, if not days in the validation cycle. Both mid-bus probes and slot interposer probes are available for Gen3 measurements.

The Agilent E2960B Series PCI Express protocol analyzer has the industry's fastest lock time of 3 to 5 fast training sequences for reliable data capture.

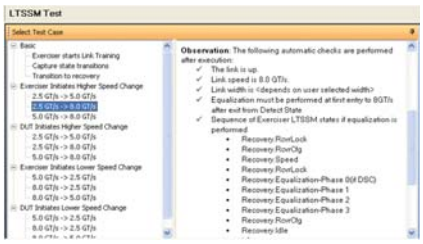


Figure 15. Over 20 pre-defined protocol error triggers to help you quickly isolate errors with the N5306A PCI Express protocol analyzer

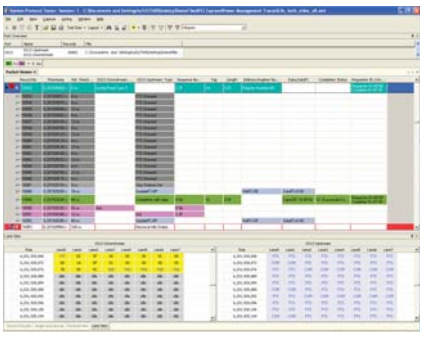
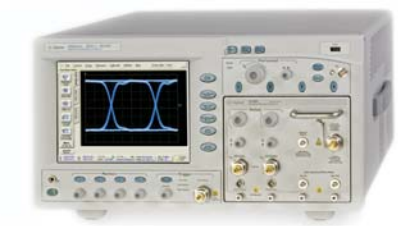


Figure 16. Multiple views of packet decode or lane view provide quicker debugging with the PCI Express protocol analyzer

Figure 17. The N4240 Series mid-bus probes feature Soft Touch technology for non-invasive probing

86100C Infiniium DCA-J wide-bandwidth oscilloscope with TDR



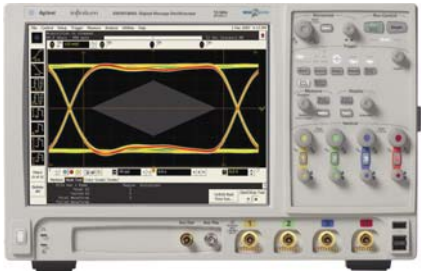
The Agilent 86100C Infiniium DCA-J combines precision waveform analysis, jitter measurements, and TDR and S-parameter measurements with one-button ease-of-use. The Agilent 86108A precision waveform analyzer provides ultra-low jitter measurements with integrated hardware clock recovery for accurate PLL analysis. The Agilent 54754A differential TDR/TDT module provides real-time impedance and crosstalk measurements.

Advanced Design System (ADS)

Agilent Technologies

With a complete set of simulation technologies ranging from frequency-, time-, numeric and physical domain simulation to electromagnetic field simulation, ADS lets designers fully characterize and optimize designs. The single, integrated design environment provides system, circuit, and electromagnetic simulators, along with schematic capture, layout, and verification capability -- eliminating the stops and starts associated with changing design tools in mid-cycle.

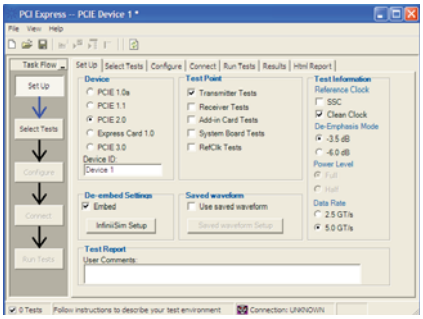
90000 Series Infiniium 13 GHz bandwidth oscilloscope



The Agilent 90000 Series Infiniium oscilloscopes deliver the highest performance real-time measurement system available. The Infiniium 90000 Series offers the industry's lowest noise floor, jitter noise floor, and trigger jitter, making it the ideal tool for signal integrity and jitter measurements. Models are available from 2.5 GHz to 13 GHz, and can be upgraded in bandwidth for future needs. The E2688A high-speed serial data analysis software and N5400A EZJIT Plus jitter analysis software provide the tools to analyze PCI Express waveforms.

EDN INNOVATION
Honoring Excellence in Electronics
WINNER 2008

N5393C PCI Express electrical compliance test software

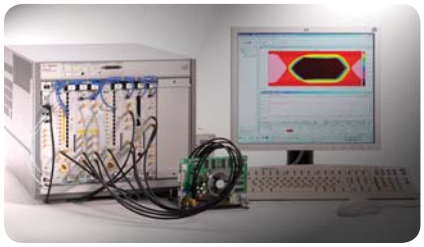


The Agilent N5393C PCI Express electrical performance validation and compliance software for the Infiniium 90000 Series oscilloscope provide a fast and easy way to verify and debug your PCI Express designs. The PCI Express electrical test software allows you to automatically execute electrical checklist tests and displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your design passed or failed each test.

J-BERT N4903B high-performance serial BERT

The J-BERT N4903B is the ideal solution for the design and test of digital components, devices and subsystems up to 12.5 Gb/s. It provides complete, calibrated jitter sources for stressed eye testing of receivers. Automated jitter tolerance testing allows quick and accurate compliance and characterization testing. For transmitter analysis, a wide range of error, eye and jitter analysis tools are built-in and provide insight into the underlying causes behind bit errors.

81250 ParBERT modular BERT platform

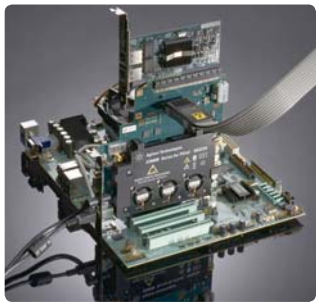


The Agilent 81250 ParBERT is a modular BERT platform for clock, data generation and data analysis up to 13.5 Gb/s that allows configuring a solution with up to 64 output and input channels that offers a PCI Express multi-lane receiver compliance test suite with the highest accuracy. The N5990A test automation software completely automates PCI Express compliance testing with the J-BERT, ParBERT and other Agilent instruments.

E2960B PCI Express protocol analyzer and exerciser

The Agilent E2960B family provides the validation and verification solution for PCI Express protocol testing. The exerciser makes it possible to validate key parts of the PCI Express design, include Link Training and Status State Machine (LTSSM), Link and Transaction Layer, Power management states, as well as performance validation. The protocol analyzer tools in the E2960B family help debug interoperability issues. The dedicated E2969A/B protocol test cards provide low cost protocol compliance test.

N5323A PCI Express jammer



The Agilent N5323A PCI Express Jammer is an innovative inline error injection tool that helps ensure your design is robust and interoperable. Validate the hardware and software under extreme conditions by creating corner cases and injecting inline errors, in a real system with any operating system, driver or application. Easy to setup, the Jammer is transparent to the PCI Express hierarchy. Just insert it into a working system, and start testing.

Agilent PCI Express Design and Test Solutions

Product	Description	PCI Express technology supported		
		1.X	2.0	3.0
	Physical Layer			
DSA90604A	6 GHz Infiniium oscilloscope	X		
DSA91304A	13 GHz Infiniium oscilloscope	X	X	X
N5393C	PCI Express electrical compliance test application	X	X	X
86100C, 86108A	DCA-J Infiniium oscilloscope with 86108A Precision waveform analyzer	X	X	X
N4916A	De-emphasis signal converter		X	X
81250	ParBERT modular BERT system	X	X	X
N5990A	Automated compliance and device characterization test software	X	X	X
86100C, 54754A	DCA-J Infiniium oscilloscope with TDR module	X	X	X
N5230C	PNA-L network analyzer	X	X	X
N1930B	Physical layer test system software (PLTS)	X	X	X
W2212B	ADS Design Software bundle (ADS Core, Transient Convolution, Layout, Momentum G2, EMDS, Ptolemy)	X	X	X
	Data link/transaction Layer			
E2960	PCI Express protocol test solution	X	X	
U4300	Digital test console			X
N5323A	PCI Express jammer	X	X	
E2969A	PCI Express 1.x protocol test card	X		
E2969B	PCI Express 2.0 protocol test card		X	

Figure 18. Agilent PCI Express solutions by technology

Related Literature

Publication title	Publication type	Publication number
90000 Series Infiniium Oscilloscope and InfiniiMax Probing System	Data Sheet	5989-7819EN
N5393B PCI Express Electrical Characterization and Compliance Software	Data Sheet	5989-1240EN
86100C Infiniium DCA-J Wide Bandwidth Oscilloscope with TDR	Data Sheet	5989-0278EN
86100CU-400 Phase Locked Loop (PLL) and Jitter Spectrum Measurement Software	Data Sheet	5989-9319EN
J-BERT N4903B High Performance Serial BERT	Data Sheet	5990-3217EN
N4916A De-Emphasis Signal Converter	Data Sheet	5989-6062EN
81250 ParBERT Modular BERT System	Product Overview	5968-9188E
N5990A Automated Compliance and Device Characterization Test Software	Data Sheet	5989-5483EN
E2960B PCI Express Protocol Tools	Data Sheet	5989-5660EN
N5323A PCI Express Jammer	Brochure	5990-3222EN
E2969A Protocol Test Card for PCI Express 1.x	Data Sheet	5989-9520EN
E2969B Protocol Test Card for PCI Express 2.0	Data Sheet	5989-7594EN
N5230C PNA-L Network Analyzer	Data Sheet	5989-7608EN
N1930B Physical Layer Test System Software (PLTS)	Data Sheet	5989-6841EN
Designing for Signal Integrity with Advanced Design System	Data Sheet	5989-8392EN
PCI Express Revision 2 Receiver Jitter Tolerance Test	Application Note	5989-4087EN
Agilent Digital Test Console PCI Express 3.0	Data Sheet	5990-5018EN

www.agilent.com
www.agilent.com/find/pci-express

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

www.axiestandard.org
AdvancedTCA® Extensions for Instrumentation and Test (AXIe) is an open standard that extends the AdvancedTCA for general purpose and semiconductor test. Agilent is a founding member of the AXIe consortium.

www.lxistandard.org
LAN eXtensions for Instruments puts the power of Ethernet and the Web inside your test systems. Agilent is a founding member of the LXI consortium.

www.pxisa.org
PCI eXtensions for Instrumentation (PXI) modular instrumentation delivers a rugged, PC-based high-performance measurement and automation system.

Agilent Channel Partners

www.agilent.com/find/channelpartners
Get the best of both worlds: Agilent's measurement expertise and product breadth, combined with channel partner convenience.

Agilent Advantage Services

Agilent Advantage Services is committed to your success throughout your equipment's lifetime. To keep you competitive, we continually invest in tools and processes that speed up calibration and repair and reduce your cost of ownership. You can also use Infoline Web Services to manage equipment and services more effectively. By sharing our measurement and service expertise, we help you create the products that change our world.

www.agilent.com/find/advantageservices

DEKRA Certified ISO 9001:2008 Quality Management System
www.agilent.com/quality

Further information on Agilent's PCI Express solutions can be found online at **www.agilent.com/find/pci-express**

Have questions about PCI Express design and test? Consult the Agilent discussion forum online at **www.agilent.com/find/forums**

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas	
Canada	(877) 894 4414
Brazil	(11) 4197 3500
Mexico	01800 5064 800
United States	(800) 829 4444

Asia Pacific	
Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 375 8100

Europe & Middle East	
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700*
	*0.125 €/minute
Germany	49 (0) 7031 464 6333
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
United Kingdom	44 (0) 131 452 0200

For other unlisted countries:
www.agilent.com/find/contactus

Revised: June 8, 2011

Product specifications and descriptions in this document subject to change without notice.

Published in USA, October 10, 2011
5989-5594EN

Agilent Technologies